

Bottleneck of using single memristor as a synapse and its solution

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the date of receipt and acceptance should be inserted later

Abstract Physical realization of the first memristor by researchers at Hewlett Packard (HP) labs attracts so much interest in this newly found circuit element which has so many applications specially in a field of neuromorphic systems. Now, it is well known that one of the main applications of memristor is for the hardware implementation of synapses because of their capability in dense fabrication and acting as a perfect analog memory. However, synapses in biological systems have this property that by progressing in the learning process, variation rate of the synapses weights should decrease which is not the case in the currently suggested memristor-based structures of neuromorphic systems. In this paper, we show that using two dissimilar memristors connected in series as a synapse perform better than the single memristor.

1 introduction

Publication of a paper [1] in Nature by HP labs in May 1, 2008, which announced the first experimental realization of the memristor whose existence was predicted in 1971 by Leon Chua [2] has caused an extraordinary increased interest in this passive circuit element. A memristor is a device that, like a resistor, opposes the passage of current. But memristors also have a memory. The resistance of a memristor at any moment depends on the last voltage it experienced, so its behavior can be used to recall past voltages. One of the widely accepted applications of memristor is for the hardware implementation of synapses in neuromorphic systems. Using memristors as synapses in neuromorphic systems can offer both high connectivity and high density (through the memristor crossbar structure) which are necessary for efficient computing. Recently, a group at the University of Michigan, led by Wei Lu, has experimentally demonstrated that a hybrid system composed of complementary metal-oxide semiconductor neurons and memristor synapses can support important synaptic functions such as Spike Timing Dependent Plasticity (STDP) [3]. However, in this paper we will show that although

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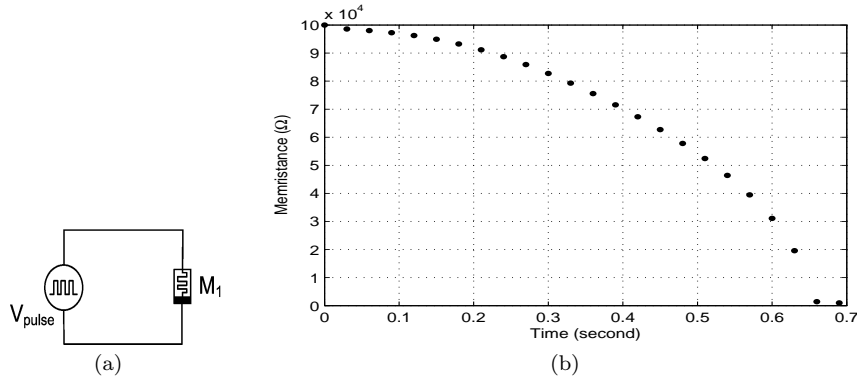


Fig. 1 (a) Simple circuit showing a single memristor connected to the pulse generator voltage source. (b) Changing of the memristance of the memristor when the series of identical positive pulses are applied to it. It is clear that later pulses change the memristance of the memristor more than the former ones.

memristor behaves so similar to the biological synapses, it has a property that makes the hardware implementation of neuromorphic systems so much complicated.

2 Bottleneck of using a single memristor as a synapse and its solution

In this section, we will show that using a single memristor as a synapse has some drawbacks. For this purpose, consider the simple circuit shown in Fig. 1(a) in which a memristor is directly connected to the pulse generator voltage source. Figure 1(b) shows that how the memristance of the memristor changes when the series of identical positive pulses are applied to it. Note that in this simulation, initial memristance of the memristor is assumed to be the highest possible value, $R_0 = R_{off} = 100k\Omega$. As expected from the DC characteristics of the memristor, the application of these positive voltage pulses incrementally decrease the memristance of the memristor. From this figure, it is evident that two identical pulses applied at different times have different impact on the memristance of the memristor: later pulses decrease the memristance more than former ones. This is because of the fact that there is a positive feedback in these kinds of circuits: application of the voltage results in a passage of the current through the memristor which decreases the memristance of it. By decreasing the memristance of the memristor, the amount of current flowing through the memristor increases which in return reduces the memristance of the memristor more.

Now consider a neuromorphic structure that this memristor maybe used in it as a synapse such as the simple one shown in Fig. 2. In this figure, two neurons are connected through the synapse represented by a memristor. Without the loss of generality, assume that the neurons are spiky and are completely correlated to each other: firing of neuron A results in a firing of neuron B. In this case and by considering any of the learning rules such as STDP, each time that both neurons fire, the connection between them should be strengthened more (Hebbian learning) which corresponds to the reduction of the memristance of the connecting memristor. Note that this statement is correct because by considering the limiting case in which there is no correlation between two neurons,

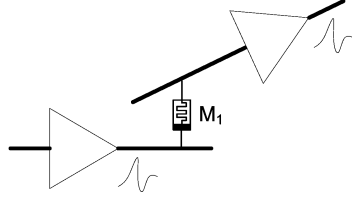


Fig. 2 Two neuron connected through the single memristor. The memristance of this memristor should be decreased when these two neurons fire Simultaneously.

there should be no connection between them which means that the memristance of the memristor should be infinity (very high). However, there is a problem in these kinds of structures which arises from the nature of the memristor as explained in previous paragraph: by proceeding in the learning process, future synapse updating pulses decrease the memristance of the memristor more than the former ones (because of the positive feedback in memristor). This may cause the system to become unstable. On the other hand in biological systems, we see the opposite case: early experiments have the most impact on learning and not the later ones (during the learning process, synapses weights change rapidly at early experiments and then they become almost stationary).

For relaxing this drawback, we propose to use the circuit shown in Fig. 3(a) as a synapse. In this figure, two dissimilar memristors with different polarities are connected in series. In fact, memristor M_1 produces the synaptic weight and is used during the computing period of the system. Memristor M_2 is added only for the removing of the mentioned problem during the updating process.

It follows from the Kirchoff's laws that if two memristors M_1 and M_2 which are connected in series have opposite polarities, their total memristance can be written as [5]:

$$M_T(q) = \left(R_{0,1} - \eta \frac{\Delta R_1 q(t)}{Q_0} \right) + \left(R_{0,2} + \eta \frac{\Delta R_2 q(t)}{Q_0} \right) \quad (1)$$

which can be rewritten as:

$$M_T(q) = (R_{0,1} + R_{0,2}) - \eta (\Delta R_1 - \Delta R_2) \frac{q(t)}{Q_0} \quad (2)$$

where:

- $R_{0,i}$ for $i = 1, 2$ is the effective memristance of the memristor M_i at time $t = 0$;
- η is the polarity of the memristor which can be +1 and -1;
- $\Delta R_i = R_{off,i} - R_{on,i} \simeq R_{off,i}$ where $R_{off,i}$ and $R_{on,i}$ are the maximum and minimum memristance values of the memristor M_i respectively;
- $q(t)$ is the amount of charge that has passed through the memristors;
- $Q_{0,i}$ is the charge that is required to pass through the memristor M_i for the dopant boundary to move through distance D where D is the total length of the memristor.

This equation shows that by connecting two memristors in series but with different polarities we can suppress the q-dependent component (second term in eq. (2)). In

addition, it is clear that the overall behavior of these memristors depends on the relationship between ΔR_1 and ΔR_2 or simply on $\alpha = \frac{\Delta R_1}{\Delta R_2}$. By properly adjusting α we can choose that how the memristance of the memristor M_1 changes relative to the applied voltage. Figures 3(a), 3(b) and 3(c) show how the memristance of the memristor M_1 varies for the various value of α when the applied voltage is 1 volt. For example, 3(b) demonstrates that when $\alpha \simeq 1$, memristance of the memristor M_1 decreases almost linearly while in the case of $\alpha \gg 1$, two memristors connected in series act similar to the single memristor (see Fig. 1(b)). Note that for performing this simulation, Spice model of memristor proposed in [4] is used and parameters $R_{off,i}$, $R_{on,i}$ and $R_{0,i}$ for $i = 1, 2$ are set to the values presented in Table 1. Comparing to Fig. 1(b), these figures indicate that when $\alpha \ll 1$, memristor M_1 becomes a perfect candidate for the hardware implementation of synapses. Note that in this case ($\alpha \ll 1$), memristance of the memristor decreases rapidly at first and then it changes slowly (similar to the weight updating mechanism in the neuromorphic systems). As a consequence, for modifying the memristance of the memristor M_1 , the updating potential should be applied between terminals 1 and 2 (in Fig. 3(a)) while during the computing period, memristor M_1 should separately be used as a synapses (utilizing terminals 2 and 3).

Table 1 Values of the memristors' parameters used for obtaining the simulation results shown in Fig. 3

α	$[R_{0,1}, R_{0,2}]$	$[R_{on,1}, R_{on,2}]$	$[R_{off,1}, R_{off,2}]$
0.01	$[9k\Omega, 9k\Omega]$	$[100\Omega, 100\Omega]$	$[10k\Omega, 1M\Omega]$
1	$[399k\Omega, 1k\Omega]$	$[100\Omega, 100\Omega]$	$[400k\Omega, 400k\Omega]$
100	$[950k\Omega, 1k\Omega]$	$[100\Omega, 100\Omega]$	$[1M\Omega, 10k\Omega]$

3 conclusion

In this paper we showed that using memristor as a synapse has this drawback that by proceeding in the learning process, variation rate of the synaptice weights increases. To solve this problem, we proposed to use two dissimilar memristors connected in series instead of one memristor as a synapses. Simulation results show that by properly adjusting parameters of these memristors, we can force the variation rate of the synaptic weights to decrease during the learning process.

References

1. D.B. Strukov, G.S. Snider, D.R. Stewart and R.S. Williams, "The missing memristor found," Nature, 2008, vol. 453, pp. 80–83, 1 May 2008.
2. L.O. Chua, "Memristor - the missing circuit element," IEEE Trans. on Circuit Theory, vol. CT-18, no. 5, pp. 507–519, 1971.
3. S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," Nano Letter, 2010, 10(4), pp. 1297–1301.
4. D. Birolek, Z. Birolek and V. Biolkova, "SPICE Modeling of Memristive, Memcapacitive and Meminductive Systems," European Conference on Circuit Theory and Design (ECTD2009), pp. 249–252, Antalya, 23–27 August 2009.
5. Y. N. Joglekar, S. J. Wolf, "The Elusive Memristor: Properties of Basic Electrical Circuits," European Journal of Physics, Vol. 30, no. 4, pp. 661–675, 2009.

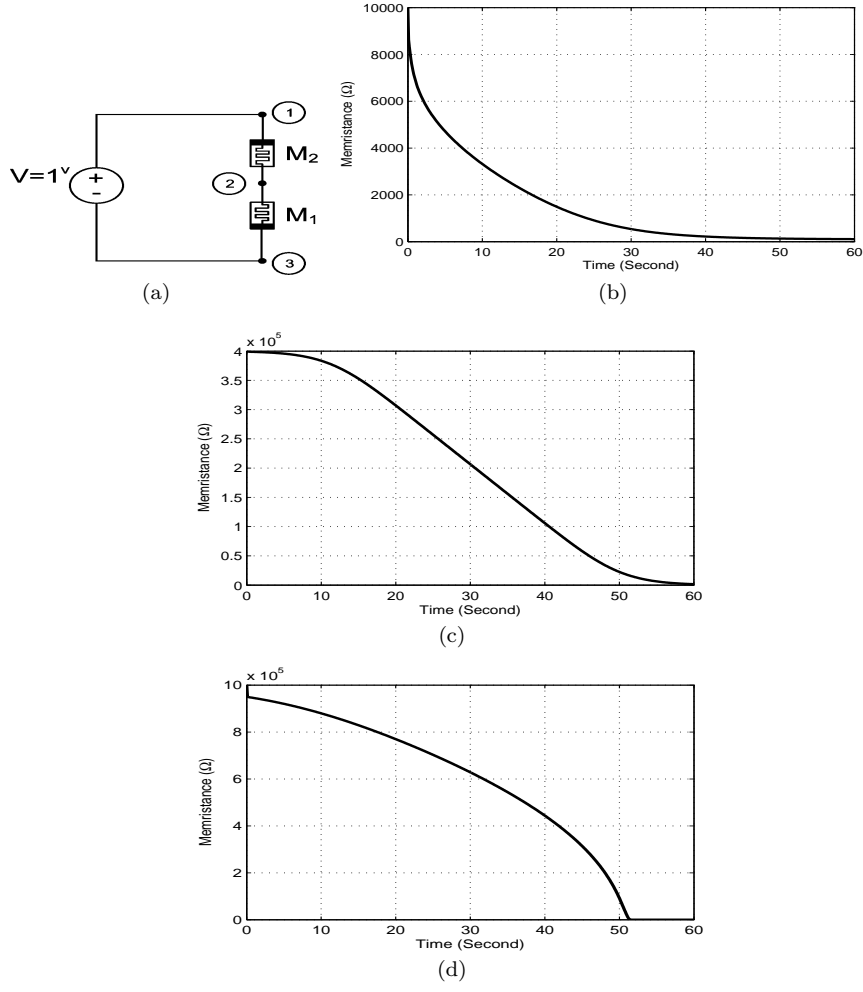


Fig. 3 (a) Our proposed circuit for using as a synapse consists of two memristors connected in series; (b) Decreasing style of the memristance of the memristor M_1 when $\alpha \ll 1$; (c) Decreasing style of the memristance of the memristor M_1 when $\alpha \simeq 1$; (d) Decreasing style of the memristance of the memristor M_1 when $\alpha \gg 1$;